REMARKS

These remarks are in reply to the Office Action mailed June 20, 2007. Claims 1-7, 10-18, 21-29, 32-33, and 37-42 stand rejected under 35 U.S.C. §102(b) as being anticipated by U.S. Pat. to Wollan et al.[1] ("Wollan"). In addition, claims 1-7, 10-18, 21-29, 32-33, and 37-42 stand rejected under 35 U.S.C. §102(b) as being anticipated by U.S. Pat. to Potter, et al.[2] ("Potter").

Applicant thanks Examiner Elmore for an interview held on September 13, 2007.

Claims 12, 23, and 37 have been amended to clarify the claimed subject matter. New claims 43-50 have been added. In addition, claim 42 has been cancelled. Applicant respectively traverses the rejections.

A. Anticipation

"A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." [3] "The identical invention must be shown in as complete detail as is contained in the ... claim."[4] In addition, the elements must be arranged as required by the claim.[5] It is "error to treat the claims as a mere catalog of separate parts, in disregard of the part-to-part relationships set forth in the claims that give those claims their meaning."[6] Moreover, a reference does not anticipate "simply by possessing identically named parts, unless these parts also have the same structure or otherwise satisfy the claim limitations, and were understood to function in the same way by one skilled in the art."[7]

To anticipate, a prior art reference need not expressly disclose particular element as set forth in the claim "if that element is 'inherent' in its disclosure."[8] "To establish inherency, the extrinsic evidence 'must make clear that the missing descriptive matter is necessarily present in the thing described in the reference,

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[1] No. 5,809,327
[2] No. 5,170,477
[3] MPEP 2131, *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987).
[4] MPEP 2131, *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).
[5] MPEP 2131, *In re Bond*, 910 F.2d 831, 15 USPQ2d 1566 (Fed. Cir. 1990).
[6] Harmon, Patents and the Federal Circuit, 4th ed., p.74, citing *Lindeman Maschinenfabrik v. American Hoist & Derrick Co.*, 730 F.2d 1452, 221 USPQ 481 (Fed. Cir. 1984).
[7] Applied Med. Res. Corp. v. United States Surgical Corp., 147 F.3d 1374, 47 USPQ2d 1289 (Fed. Cir. 1998).
[8] *In re Robertson,* 169 F.3rd 743, 49 USPQ2d 1949 (Fed. Cir. 1999).

and that it would be so recognized by persons of ordinary skill. Inherency, however, may not be established by probabilities or possibilities. The mere fact that a certain thing may result from a given set of circumstances is not sufficient.' "[9] With regard to process claims, "if a prior art device, in its normal and usual operation, would necessarily perform the method claimed, then the method claimed will be considered to be anticipated by the prior art device."[10] Moreover, "in relying upon the theory of inherency, the examiner must provide a basis in fact and/or technical reasoning to reasonably support the determination that the allegedly inherent characteristic necessarily flows from the teachings of the applied prior art."[11]

B. Rejection of Claims

37 CFR §1.104 (c) (2) provides that "in rejecting claims for want of novelty or for obviousness, the examiner must cite the best references at his or her command. When a reference is complex or shows or describes inventions other than that claimed by the applicant, the particular part relied on must be designated as nearly as practicable. The pertinence of each reference, if not apparent, must be clearly explained and each rejected claim specified."

C. Claim 1 recites "(c) producing a first count of address-bytes received on the bus as a result of receiving the first address-byte." According to the Office Action, Wollan discloses this limitation at col. 4, line 62 to col. 5, line 20. Wollan is both a complex reference, and one which describes subject matter which is not particularly pertinent to applicant's claims.

First, Wollan discloses, in the material cited in the Office action, that "to facilitate memory access, certain sixteen bit arithmetic operations, such as post-increment and pre-decrement, are provided for address calculations." (col. 5, lines 13-16.) In the next paragraph, an arithmetic and logic unit ALU-2 is disclosed. This particular part is "a sixteen bit design, customized to provide specific operations typically required of indirect address pointers" (col. 5, lines 24-26), which has a first input which is fed by the sixteen-line data-out bus 104 and a second input which is fed by a selector 110. (col. 5, lines 26-28.) However, Wollan

[9] MPEP 2112 IV., citing *In re Robertson.* See also Ex Parte Mary Smith, BAPI 2007-1925 (2007).
[10] MPEP 2112.02
[11] MPEP 2112 IV., citing *Ex parte Levy,* 17 USPQ2d 1461, 1464 (Bd. Pat. App. & Inter. 1990) (emphasis in original).

does not disclose, in this citation, that this customized part counts the number of addresses received on the sixteen-bit bus. One of ordinary skill in the art would recognize that the Wollan ALU-2 performs operations on the contents of registers it is coupled with via the sixteen-bit bus. As applicant has previously pointed out, "incrementing the *content* of a logical register is not equivalent to incrementing a count whenever a byte is received."[12] It cannot be said that the ALU-2, coupled with the sixteen-bit bus and the selector 110, in its normal and usual operation, would necessarily perform a step of counting the number of addresses received on the sixteen-bit bus. The mere fact that this particular part could, if configured differently, perform the claimed step is not sufficient to support a finding of anticipation.

Second, Wollan discloses in this citation "two sixteen-line data buses 102, 104" (col. 5, lines 3-4.) These two busses are "for the sixteen bit registers" R27/R26, R29/R28, R31/R30. The sixteen bit registers "are used as indirect address register pointers for RAM and program-space addressing." (col. 5, lines 11-13.) How large is the address space? Wollan states "whether for data or for program memory, a 16-bit address space greatly increases the flexibility and utility of the microcontroller by increasing both the program address space and the data address space." (col. 2, lines 22-24.) Thus, the particular part cited in the Office Action is a sixteen-line data bus which is used to access a 16-bit address space. However, this teaching does not correspond with the bus recited in the portion of claim 1 quoted above. The preamble to claim 1 recites "an N-bit bus, where M is greater than N," where M refers to a memory space having 2^M addresses. Plainly, the bus recited in the claim is an N-bit bus, whereas the particular Wollan bus cited in the Office Action is an M-bit bus. It is true that Wollan elsewhere discloses an 8-bit data bus. But Wollan discloses that the ALU-2 is only coupled with 16-bit busses. For example, Wollan does not disclose that the ALU-2 is directly coupled with the 8-bit data bus 12. It follows that if the particular part cited in the Office Action for performing the step of producing a first count of address-bytes is not in communication with the N-bit bus on which the first address-byte is received, the particular part, even if capable of performing the step, does not expressly or inherently describe the step.

[12] Response B, p. 15, first paragraph.

Wollan also discloses an eight-bit ALU-1 coupled with an eight-bit data bus 12. While the Office Action correctly does not rely on the ALU-1 as a disclosure of the step of producing a first count of address-bytes received on the bus, applicant notes that this particular part cannot be relied on for such disclosure. Wollan does not disclose that the ALU-1 necessarily performs a step of counting the number of addresses received on the eight-bit bus. Like the ALU-2, the mere fact that this particular part could, if configured differently, perform the claimed step is not sufficient to support a finding of anticipation.

The Office Action states that the step (c) of producing a first count is "as the system *keeping track* of the first half of the 16 bit logical address otherwise the system would not place the second half of the 16 bit logical address in the correct register," citing col. 4, line 62 to col. 5, line 20. The cited text discusses the REGISTER FILE, including the 16-bit logical registers, but is silent with respect to how the particular registers are identified or selected. The cited text does not discuss the problem of keeping track of 8-bit halves of a logical 16-bit address or how the problem could be solved. Accordingly, there is no explicit basis cited in the Office Action for the examiner's argument. Applicant agrees that one of ordinary skill in the art would recognize that keeping track of 8-bit halves is a problem that the Wollan microcontroller must somehow address. There are two possibilities. First, a solution to the problem of keeping track of 8-bit halves of a logical 16-bit address could be described elsewhere in this complex reference. Or the argument expressed in the Office Action is premised on inherency, i.e., that the Wollan reference inherently discloses producing a first count of address-bytes received on the N-bit bus.

As to the first possibility, applicant refers the examiner to Response A filed in this matter, pages 10-12. In Response A, it was pointed out in some detail that Wollan discloses selector control circuitry 134 having as inputs a plurality of control lines. Wollan states: "consider, for example, the writing of data into register R0. The five bit control line R_SEL is set to select register R0. The decoder 140 decodes the line, thereby asserting the output line corresponding to register R0."[13] Thus, Wollan is explicit: selector control circuitry 134 is employed to select

[13] Wollan, col. 7, lines 52-54 (emphasis added).

particular registers in the REGISTER FILE, and selects a particular register according to control signals on the control lines.

Wollan explains that program instructions "are decoded by an INSTRUCTION DECODER which generates various control signals. The control signals are carried by CONTROL LINES to the other components of the microcontroller 10 to perform operations in accordance with decoded program instructions." (col. 4, lines 36-38.) Indeed, claim 1 is directed to "a microcontroller comprising . . . an instruction execution unit having a plurality of control lines for providing control signals in response to execution of an instruction." Wollan notes various "control signals are pertinent to the operation of the discussed features of the REGISTER FILE," explaining that "these signals are carried by various CONTROL LINES originating from the INSTRUCTION DECODER." (col. 5, lines 39-47.) Table I of the Wollan reference summarizes the control lines which control the microcontroller to implement the instruction set. From the foregoing it is clear that the control signals that are used to direct the selector control circuitry 134 to select a particular register originate in program instructions. Thus, Wollan does not disclose that the problem of keeping track of 8-bit halves of a logical 16-bit address is solved in the disclosed hardware. If the problem is solved at all, the solution must be found in particular program instructions. Wollan discloses the instruction set of the microcontroller beginning at col. 11, line 64, but is silent as to how the specific program instructions could be used to solve the problem of keeping track of 8-bit halves of a logical 16-bit address. Therefore, the argument expressed in the Office Action must be that the Wollan *inherently* discloses producing a first count of address-bytes received on the N-bit bus.

The Office Action provides no basis to reasonably support a determination that the step of "producing a first count of address-bytes received on the bus as a result of receiving the first address-byte" necessarily flows from the teachings of the Wollan reference. The Office Action does not show that the Wollan microcontroller, in its normal and usual operation, would necessarily perform a step of "producing a first count of address-bytes received on the bus."

Accordingly, Wollan does not, either expressly or inherently, describe the step of "(c) producing a first count of address-bytes received on the bus as a result of receiving the first address-byte" Moreover, the conclusion stated above that "that

the ALU-2, in its normal and usual operation, would necessarily perform a step of counting the number of addresses received on the sixteen-bit bus" is reinforced by the Wollan disclosure that the problem of keeping track of 8-bit halves of a logical 16-bit address is solved in the disclosed hardware.

Claim 1 also recites "(d) selecting a first one of the at least two registers, the first register corresponding with the first count." According to the Office Action, Wollan discloses this limitation at col. 4, line 47 to col. 5, line 20. The only discussion of *selecting* found in the material cited in the Office Action is with respect to discussion of an eight bit ALU-1. This part provides "eight bit arithmetic operations between registers *selected* from the REGISTER FILE. The output of ALU-1 can be fed back to a register in the REGISTER FILE via the data bus 12." (col. 4, lines 52-56.) However, this material cited in the Office Action is silent as what part does the selecting and on what basis a selection is made. A disclosure that a thing performs some operation with respect to a selected register *after a selection has been made*, is clearly distinct from a disclosure of a thing performing a step of selecting. Thus, the Office Action does not point out where the Wollan reference discloses the step of selecting a first one of the registers.

Step (d) includes a limitation that the first register corresponds with the first count. Plainly, this limitation indicates how the first register is identified. However, there is no discussion whatsoever in the material cited in the Office Action with respect to step (d) of how registers in the REGISTER FILE are identified. Accordingly, the Office Action does not explain how Wollan discloses this limitation.

D. Amended claim 12 is directed to an apparatus that comprises at least two registers. The claim includes the limitation that "each register is associated with a particular count of address-bytes received on the bus." According to the Office Action, this limitation is disclosed by Figure 1, element 20. There is no disclosure in Figure 1 of Wollan that indicates how the registers 20 are identified. Moreover, there is no disclosure in the Wollan reference that any register is associated with a particular count value.

Amended claim 12 recites "an N-bit bus, where M is greater than N." According to the Office Action, this limitation is disclosed at col. 1, lines 38-57. The

cited language from Wollan explains that certain "microcontrollers use the Harvard dual-bus architecture where data and program instructions have separate memories and buses." There are no other references to buses in the text cited in the Office Action. Accordingly, the cited language does not provide a reasonable basis for concluding that the claimed N-bit bus is disclosed by the Wollan reference.

Amended claim 12 recites "a logic circuit coupled with the bus, the first and second control signal lines, and the at least two registers, the logic circuit to select one of the at least two registers." The claimed logic circuit, according to the Office Action, is disclosed by the program counter, the program flash, the instruction register, which Wollan collectively refers to as "instruction execution components," and instruction decoder shown in Figure 1, and the at least two registers are disclosed by the register file 20. First, the claimed logic circuit is coupled with the claimed N-bit bus. None of the instruction execution components are coupled with an N-bit bus. Figure 1 clearly shows that the instruction execution components are coupled only with busses 14, 16, and control lines. As described above, Wollan has a memory space of 2^{16} addresses. Wollan discloses that the busses 14, 16 are both 16-bit busses (see Figures 1 and 12). Therefore, Wollan does not disclose that the instruction execution components are coupled with an N-bit bus. Rather, it discloses that the instruction execution components are coupled with an M-bit bus.

Amended claim 12 recites that the logic circuit includes an address-byte-received counter, which is disclosed at col. 4, lines 62 to col. 5, line 20 of Wollan according to the Office Action. As noted above with respect to claim 1, the only reference to counting in the cited text in Wollan is that "to facilitate memory access, certain sixteen bit arithmetic operations, such as post-increment and pre-decrement, are provided for address calculations." (col. 5, lines 13-16.) As mentioned the next paragraph discloses the ALU-2 part. Moreover, there is no discussion whatsoever in the cited text of the "instruction execution components." Thus, there is no reasonable basis in the material cited in the Office Action to support a conclusion that the "instruction execution components," which the Office Action maintains correspond with the claimed logic circuit, includes an address-byte-received counter.

In addition, with respect the claimed address-byte-received counter, the Office action states repeats the statement "the system *keeping track* of the first half

of the 16 bit logical address otherwise the system would not place the second half of the 16 bit logical address in the correct register." As explained above, this is an argument that Wollan *inherently* discloses the claimed address-byte-received counter. The Office Action provides no basis conclude the missing address-byte-received counter is necessarily present in the microcontroller described in Wollan, and that it would be so recognized by persons of ordinary skill.

E. Amended claim 23 is directed to a machine readable medium embodying a program of instructions for execution by a machine to perform a method for high speed addressing of a memory space having 2^M addresses using an N-bit bus. Applicant's arguments made with respect to claim 1 are equally applicable to claim 23. Amended claim 23 is not anticipated by Wollan for at least the same reasons the claim 1 is not anticipated by Wollan.

F. Amended claim 37 is directed to a system. Applicant's arguments made with respect to claim 12 are equally applicable to claim 37. Amended claim 37 is not anticipated by Wollan for the at least same reasons the claim 12 is not anticipated by Wollan.

G. Accordingly, the Wollan reference fails to disclose each and every element of independent claims 1, 12, 23, and 37.

H. Claims 1 stands rejected as being anticipated by Potter. According to the Office Action, the Potter reference discloses the limitation in section (a) of claim 1 that each register is "associated with a particular count of address-bytes received" on the N-bit bus at col. 3, line 53 to col. 4, line 30. However, the only reference in this paragraph to counting is to "a counter 40 for keeping count of the data item(s) temporarily stored in the DMA controller." (emphasis added.) Plainly, the cited text does not *expressly* disclose counting anything received on a bus outside of the DMA controller. In particular, there is not the slightest hint in the cited text that one of the Potter registers is associated with a count.

According to the Office Action, Figure 1 discloses an N-bit bus. According to claim 1, a memory space having 2^M addresses is addressed with an N-bit bus, where M is greater than N. However, an N-bit bus is not disclosed in Figure 1 of Potter. To the contrary, Potter discloses transferring data items in a memory space having 2^M addresses using an M-bit bus. (col. 5, lines 57-60.) Potter also discloses

that the 32-bit data bus includes four parallel 8-bit lines, that data may be transferred on one or more of the four 8-bit lines, and that a source/destination may be a 32-bit, 16-bit, or an 8-bit sized device. (col. 4 lines 11-25.) Thus, if a destination space is 32-bits a 32-bit bus is used, if a destination space is 16-bits a 16-bit bus is used, and if a destination space is 8-bits an 8-bit bus is used.

Claim 1 includes "(c) producing a first count of address-bytes received on the bus as a result of receiving the first address-byte." According to the Office Action, this limitation corresponds with the DMA controller determining "the first address of the amount (*sic*) of data being requested" as disclosed at col. 3, line 53 to col. 4, line 30. Applicant discerns no discussion, however, in the cited text with respect to such a determination. Applicant will assume that the examiner intended to refer to the text at col. 3, lines 47-58, which provides:

"In order to transfer a data block from the source device (e.g., a first memory) to the destination device (e.g., a second memory), *the DMA controller must receive a starting or initial address or storage location of the source device*, which starting address corresponds to the address in which the first byte of data to be transferred is located, *along with the total amount of data* (e.g., the total number of bytes) *to be transferred.* In the case where the destination device is a memory, *the DMA controller also needs to receive that address location of the destination device where the first byte of data transferred* from the source device *is to be stored.*"

However, there is no reference in this passage to producing a count. Receiving an address does not *expressly* describe producing a count of address-bytes received on an N-bit bus. Nor does receiving a quantity of bytes to be transferred *explicitly* describe producing a count of address-bytes received on an N-bit bus. If the Office Action intends that the Potter text at col. 3, lines 47-58 *inherently* describes what is claimed, the examiner must provide a basis in fact and/or technical reasoning to reasonably support the determination that the allegedly inherent characteristic necessarily flows from the teachings of the applied prior art. If the examiner intends to refer to description in the Potter reference other than that assumed by applicant, it is respectfully requested that the examiner designate the particular text, drawing, or part relied as nearly as practicable.

Limitation (d) of claim 1, according to the Office Action, corresponds with "selecting the registers within the buffer for a selected memory operation," as disclosed at col. 3, line 53 to col. 4, line 30. Again Applicant discerns no discussion whatsoever in the cited text with respect to "selecting the registers within the buffer for a selected memory operation." Applicant agrees that the Potter reference discloses that registers within the buffer are selected. See Figure 3(B), for example. Indeed, it appears that a particular Potter register is selected because of its correspondence with one of the four parallel 8-bit lines of the data out bus. However, the claim language is specific: a first one of the at least two registers is selected because the first register corresponds with a first count of address-bytes received on the N-bit bus. Accordingly, based on the text cited in the Office Action and applicant's reading of the Potter reference, there is not even the slightest suggestion that Potter discloses limitation (d) of claim 1. If the examiner intends to refer to description in the Potter reference other than Figure 3(B) as assumed by applicant, it is respectfully requested that the examiner designate the particular text, drawing, or part relied as nearly as practicable.

I. Claim 12 stands rejected as being anticipated by Potter.

According to the Office Action, the Potter reference discloses that each register is "associated with a particular count of address-bytes received" on the N-bit bus. For the reasons stated above in section H., Applicant disagrees. The Potter reference does not disclose registers are associated with a particular count.

According to the Office Action, Potter discloses an N-bit bus, where M is greater than N. As noted in section H, Potter clearly discloses that if a destination space is 32-bits a 32-bit bus is used, if a destination space is 16-bits a 16-bit bus is used, and if a destination space is 8-bits an 8-bit bus is used. There is simply no suggestion in Potter of an N-bit bus, where M is greater than N.

According to the Office Action, Potter discloses "an address-byte received counter to count address bytes received on the bus." As noted in section H, Potter does not *expressly* disclose counting anything received on a bus outside of the DMA controller. The counter 40 is "for keeping count of the data item(s) temporarily stored in the DMA controller." (emphasis added.)

According to the Office Action, gating circuitry 30 corresponds with the claimed selecting unit. The gating circuitry 30 is shown in detail in Figure 8. Figure 8 does not disclose that the gating circuitry 30 is responsive to a particular count of address-bytes received on a bus, as claimed.

J. Claim 23 stands rejected as being anticipated by Potter.

According to the Office Action, Potter discloses receiving a first address byte on an N-bit bus, citing Figure 1. As explained in section J, one of ordinary skill in the art would not understand that Potter describes an N-bit bus, where M is greater than N.

According to the Office Action, Potter discloses "(c) selecting a first one of the at least two registers, the first register corresponding with the first count." As explained above with reference to claim 1, section (d), based on the text cited in the Office Action and Figure 3(B) of the Potter reference, one of ordinary skill in the art would not understand that Potter describes this limitation.

K. Claim 37 stands rejected as being anticipated by Potter.

According to the Office Action, Potter discloses an N-bit bus, where M is greater than N. There is simply no suggestion in Potter of an N-bit bus, where M is greater than N. See section H. Potter clearly discloses that if a destination space is 32-bits a 32-bit bus is used, if a destination space is 16-bits a 16-bit bus is used, and if a destination space is 8-bits an 8-bit bus is used.

According to the Office Action, Potter discloses "an address-byte received counter to count address bytes received on the bus," citing figure 1, element 40. The counter 40 is "for keeping count of the data item(s) temporarily stored in the DMA controller." (emphasis added.) Potter does not *expressly* disclose counting anything received on a bus outside of the DMA controller.

L. Accordingly, the Potter reference fails to disclose each and every element of independent claims 1, 12, 23, and 37.

M. Claims 2-7, 10-11, and 43-44 depend from amended claim 1. Claims 2-7, 10-11, and 43-44 are not anticipated by the Wollan reference or by the Potter reference for the same reasons that claim 1 is not anticipated.

Claims 13-18, 21-22, and 45-46 depend from amended claim 12. Claims 13-18, 21-22, and 45-46 are not anticipated by the Wollan reference or by the Potter reference for the same reasons that claim 12 is not anticipated.

Claims 24-29, 32-33, and 47-48 depend from amended claim 23. Claims 24-29, 32-33, and 47-48 are not anticipated by the Wollan reference or by the Potter reference for the same reasons that claim 23 is not anticipated.

Claims 38-41 and 49-50 depend from amended claim 37. Claims 38-41 and 49-50 are not anticipated by the Wollan reference or by the Potter reference for the same reasons that claim 37 is not anticipated.

Conclusion

Accordingly, claims 1-7, 10-18, 21-29, 32-33, 37-41, and 43-50 are in condition for allowance. Applicant respectively requests that claims 1-7, 10-18, 21-29, 32-33, 37-41, and 43-50 be allowed, and this application be passed to issue. Should the Examiner feel that a telephone conference would expedite prosecution of this application, the Examiner is invited to call Applicant's attorney, Richard A. Wilhelm (48,786), at (503) 635-1187.

Respectfully submitted,

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